

## WHAT IS CLAIMED IS:

1           1.    An integrated circuit ("IC") simulation system operable  
2   to (i) store a plurality of Hardware Description Language ("HDL")  
3   modules, each one of said plurality of HDL modules representative  
4   of a circuit element, (ii) receive a HDL description of a circuit  
5   to be simulated, and (iii) synthesize a circuit netlist as a  
6   function of said received HDL circuit description and ones of said  
7   plurality of HDL modules, said circuit netlist defining behavioral  
8   relationships among associated ones of said ones of said plurality  
9   of HDL modules, and associate a timing-violation controller with  
10   said circuit netlist, said timing-violation controller to ignore  
11   selected timing violations sensed during simulation of said circuit  
12   as a function of ones of said defined behavioral relationships.

1           2.    The IC simulation system as set forth in Claim 1  
2   comprising a processor and associated memory.

1           3.    The IC simulation system as set forth in Claim 2 wherein  
2   said associated memory is operable to store an IC-design  
3   process program and wherein said processor is operable to execute  
4   said IC-design process program.

1           4.    The IC simulation system as set forth in Claim 2 wherein  
2   said associated memory is operable to store said circuit netlist as  
3   a data structure.

1           5.    The IC simulation system as set forth in Claim 1 wherein  
2   said each one of said plurality of HDL modules is parameterized and  
3   specifies a logical operation.

1           6.    The IC simulation system as set forth in Claim 5 further  
2   operable to selectively match, with directed acyclic graphs  
3   ("DAGs"), a logical operation of said HDL description with a  
4   parameterized HDL module that is capable of performing said logical  
5   operation.

1           7.    The IC simulation system as set forth in Claim 1 wherein  
2    said timing-violation controller operates to not ignore ones of  
3    said selected timing violations sensed during simulation of said  
4    circuit as a function of ones of said defined behavioral  
5    relationships.

1           8.    A method of operating an integrated circuit ("IC")  
2 simulation system comprising the steps of:

3                storing a plurality of Hardware Description Language  
4 ("HDL") modules in memory, each one of said plurality of HDL  
5 modules representative of a circuit element;

6                receiving a HDL description of a circuit to be simulated;

7                synthesizing a circuit netlist as a function of said  
8 received HDL circuit description and ones of said plurality of HDL  
9 modules, said circuit netlist defining behavioral relationships  
10 among associated ones of said ones of said plurality of HDL  
11 modules; and

12                associating a timing-violation controller with said  
13 circuit netlist, said timing-violation controller to ignore  
14 selected timing violations sensed during simulation of said circuit  
15 as a function of ones of said defined behavioral relationships.

1           9.    The method of operating said IC simulation system as set  
2 forth in Claim 8 wherein said IC simulation system comprises a  
3 processor that is associated with said memory.

1           10. The method of operating said IC simulation system as set  
2 forth in Claim 9 further comprising the steps of:  
3           storing an IC-design process program; and  
4           executing said IC-design process program with said  
5 processor.

1           11. The method of operating said IC simulation system as set  
2 forth in Claim 9 further comprising the step of storing said  
3 circuit netlist as a data structure.

1           12. The method of operating said IC simulation system as set  
2 forth in Claim 8 wherein said each one of said plurality of HDL  
3 modules is parameterized and specifies a logical operation.

1           13. The method of operating said IC simulation system as set  
2 forth in Claim 12 further comprising the step of selectively  
3 matching, with directed acyclic graphs ("DAGs"), a logical  
4 operation of said HDL description with a parameterized HDL module  
5 that is capable of performing said logical operation.

1           14. The method of operating said IC simulation system as set  
2   forth in Claim 8 further comprising the step of operating said  
3   timing-violation controller to not ignore ones of said selected  
4   timing violations sensed during simulation of said circuit.

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1           15. A computer readable memory that directs a computer to  
2 operate as an integrated circuit ("IC") simulation system,  
3 comprising:

4           a plurality of Hardware Description Language ("HDL")  
5 modules stored in said computer readable memory, each one of said  
6 plurality of HDL modules representative of a circuit element;

7           a HDL description of a circuit to be simulated stored in  
8 said computer readable memory;

9           executable instructions stored in said computer readable  
10 memory to synthesize a circuit netlist as a function of said HDL  
11 circuit description and ones of said plurality of HDL modules, said  
12 circuit netlist defining behavioral relationships among associated  
13 ones of said ones of said plurality of HDL modules; and

14           executable instructions stored in said computer readable  
15 memory to associate a timing-violation controller with said circuit  
16 netlist, said timing-violation controller to ignore selected timing  
17 violations sensed during simulation of said circuit as a function  
18 of ones of said defined behavioral relationships.

1           16. The computer readable memory as set forth in Claim 15  
2 further comprising an IC-design process program stored in said  
3 computer readable memory.

1           17. The computer readable memory as set forth in Claim 15  
2 wherein said circuit netlist is stored in said computer readable  
3 memory as a data structure.

1           18. The computer readable memory as set forth in Claim 15  
2 wherein said each one of said plurality of HDL modules is  
3 parameterized and specifies a logical operation.

1           19. The computer readable memory as set forth in Claim 18  
2 further comprising executable instructions stored in said computer  
3 readable memory to selectively match, with directed acyclic graphs  
4 ("DAGs"), a logical operation of said HDL description with a  
5 parameterized HDL module that is capable of performing said logical  
6 operation.



